GaN Enhancement Mode 650V Power Transistor

FET-E6007PB010

Datasheet Rev. V03

ANCORA

Confidential Level_ Public

ANCORA

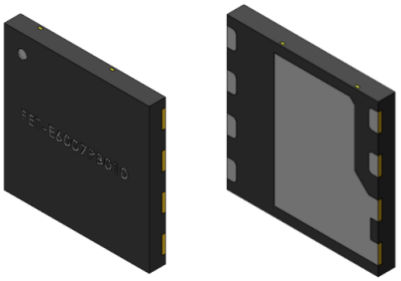
FET-E6007PB010

GaN Enhancement Mode 650V Power Transistor

1. Description

Features

- 650V E-mode GaN FET
- DFN 8x8mm

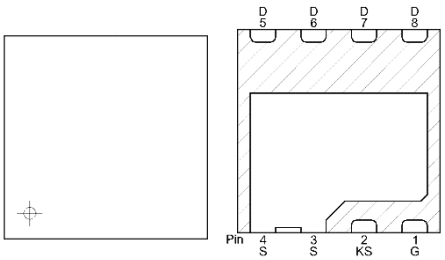


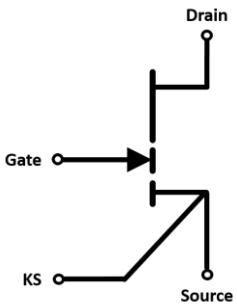
Applications

- High switching frequency converter
- High density converter

Table 1. Key Performance Parameters at T_j = 25°C

Parameter	Value	Unit
$V_{DS,\ max.}$	650	V
$R_{DS(on),\ typ.}$	65	mΩ
$Q_{G,\ typ.}$	5.38	nC
I_D Continuous drain current	21.3	A
Q_{oss} @ 400V	45	nC
Q_{rr}	0	nC
E_{oss} @ 400V	5.8	μJ





Confidential Level_ Public

2. Maximum ratings

At T_j=25°C, unless otherwise specified.

Table 2. Maximum rating

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain source voltage	V_{DS}	-	-	650	V	V_{GS}=0V
Drain source pulse voltage [1]	$V_{DS(pulse)}$	-	-	800	V	V_{GS}=0V, time≦1μs, T_j≦125°C, ≦10 million Pulses
Continuous drain current	I_D	-	-	21.3	A	T_C=25°C, T_j=150°C
		-	-	13.5	A	T_C=100°C, T_j=150°C
		-	-	9.5	A	T_C=125°C, T_j=150°C
Pulsed drain current	$I_{D, pulse}$	-	-	67.2	A	T_C=25°C, V_{GS}=6V (Duty=0.1, t_{pulse}=1μs) See Fig. 3
		-	-	30.1	A	T_C=125°C, V_{GS}=6V (Duty=0.1, t_{pulse}=1μs) See Fig. 4
Gate source voltage	V_{GS}	-10	-	7	V	Recommended operating Range: V_{GS} >=5.5V
Gate source pulse voltage	$V_{GS(pulse)}$	-	-	8.5	V	time=20ns, T_j≦125°C, ≦10 million Pulses
Power dissipation	P_{tot}	-	-	74	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	Max shelf life depends on storage conditions
Operating junction temperature	T_j	-55	-	150	°C	-
Drain source voltage slew rate	dV/dt	-	-	200	V/ns	-

[1] The allowable non-periodic VDS_pulse under abnormal operating conditions should be below 800V.
The operation for pulse number≤10 million cycles has been checked.

Confidential Level_ Public

3. Thermal characteristics

Table 3. Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC_top}	-	N/A	-	°C/W	Top case
	R_{thJC_bottom}	-	1.7	-	°C/W	Bottom case
Thermal resistance, junction-ambient for SMD version	R_{thJA}	-	45	-	°C/W	Device on 40x40x1.5mm3 single layer epoxy PCB FR4 with 6cm2 copper area (2oz.). PCB is vertical in still air.
Soldering temperature, wave soldering only allowed at leads	T_{solder}	-	-	260	°C	MSL3

4. Electrical characteristics

At T_j=25°C, unless otherwise specified.

Table 4. Static characteristics

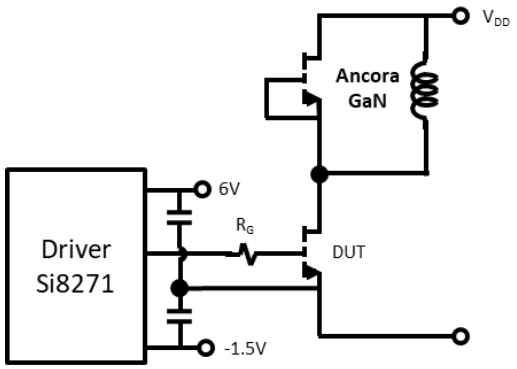
Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.0	1.52	2.6	V	V_{DS}=50mV, I_D=18mA, T_j=25°C
Drain-source leakage current	I_{DSS}	-	0.25	150	μA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
		-	20	-	μA	V_{DS}=650V, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	33	-	μA	V_{GS}=6V, V_{DS}=0V, T_j=25°C
Drain-source on-state resistance	$R_{DS(on)}$	-	67	-	mΩ	V_{GS}=5.5V, I_D=8A, T_j=25°C
		-	65	96	mΩ	V_{GS}=6V, I_D=8A, T_j=25°C
		-	64	-	mΩ	V_{GS}=6.5V, I_D=8A, T_j=25°C
		-	162.5	-	mΩ	V_{GS}=6V, I_D=8A, T_j=150°C
Source-drain reverse voltage	V_{SD}	-	2.4	-	V	V_{GS}=0V, I_D=8A, T_j=25°C

Confidential Level_ Public

Table 5. Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	199.9	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
Output capacitance	C_{oss}	-	49.4	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
Reverse transfer capacitance	C_{rss}	-	0.4	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
Effective output capacitance, energy related [2]	$C_{o(er)}$	-	72.5	-	pF	V_{GS}=0V, V_{DS}=0V to 400V
Effective output capacitance, time related [3]	$C_{o(tr)}$	-	112.5	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0V to 400V
Output charge	Q_{oss}	-	45	-	nC	V_{GS}=0V, V_{DS}=0 to 400V
Turn-on delay time [4]	$t_{d(on)}$	-	2.34	-	ns	V_{DS}=400V, V_{GS}=6V/-1.5V, I_D=8A, R_G=5Ω
Rise time [4]	t_r	-	3.35	-	ns	V_{DS}=400V, V_{GS}=6V/-1.5V, I_D=8A, R_G=5Ω
Turn-off delay time [4]	$t_{d(off)}$	-	10.46	-	ns	V_{DS}=400V, V_{GS}=6V/-1.5V, I_D=8A, R_G=5Ω
Fall time [4]	t_f	-	6.11	-	ns	V_{DS}=400V, V_{GS}=6V/-1.5V, I_D=8A, R_G=5Ω
Gate resistance	R_G	-	0.9	-	Ω	f=100MHz, open drain

[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.
[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V.
[4] Test circuit:



Confidential Level_ Public

Table 6. Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	0.8	-	nC	V_{DS}=400V, I_D=8A, V_{GS}=0 to 6V
Gate to drain charge	Q_{GD}	-	1.78	-	nC	V_{DS}=400V, I_D=8A, V_{GS}=0 to 6V
Gate charge total	Q_G	-	5.38	-	nC	V_{DS}=400V, I_D=8A, V_{GS}=0 to 6V
Gate plateau voltage	$V_{plateau}$	-	2.3	-	V	V_{DS}=400V, I_D=8A, V_{GS}=0 to 6V

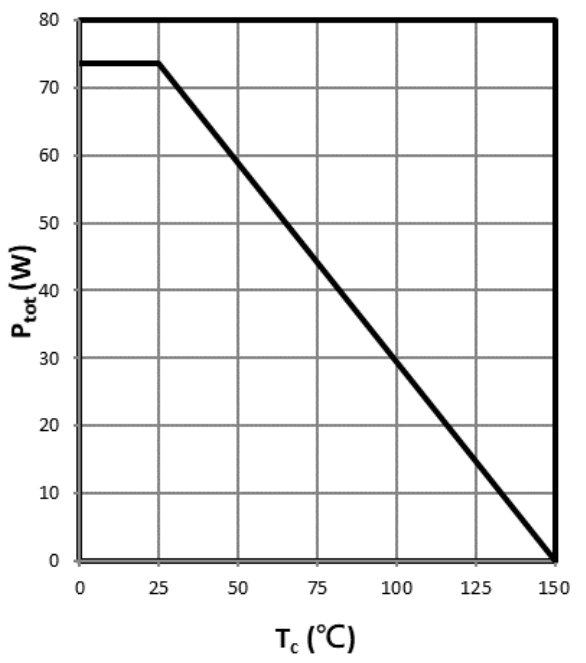
Table 7. Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Pulsed current, reverse	$I_{s,\ pulse}$	-	-	67.2	A	Tc=25°C
Reverse recovery chart	Q_{rr}	-	0	-	nC	Excluding Qoss
Reverse recovery time	T_{rr}	-	0	-	nS	-
Peak reverse recovery current	I_{rrm}	-	0	-	A	-

Confidential Level_ Public

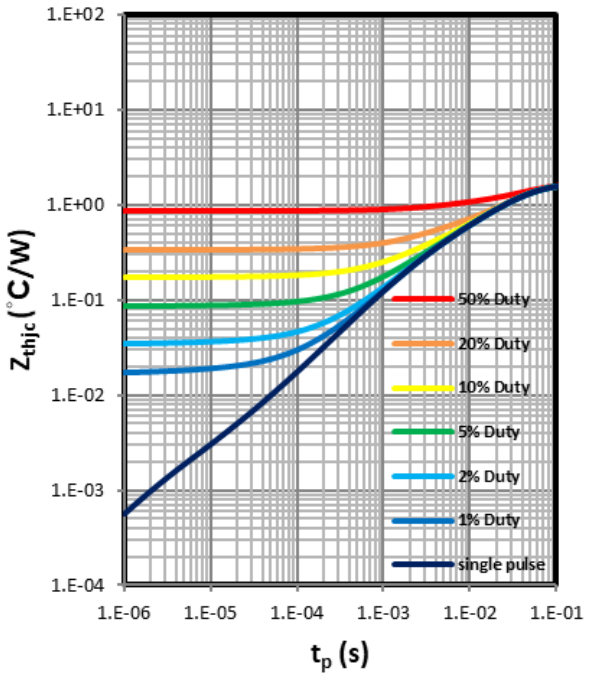
5. Electrical characteristics diagrams

Fig 1. Power dissipation



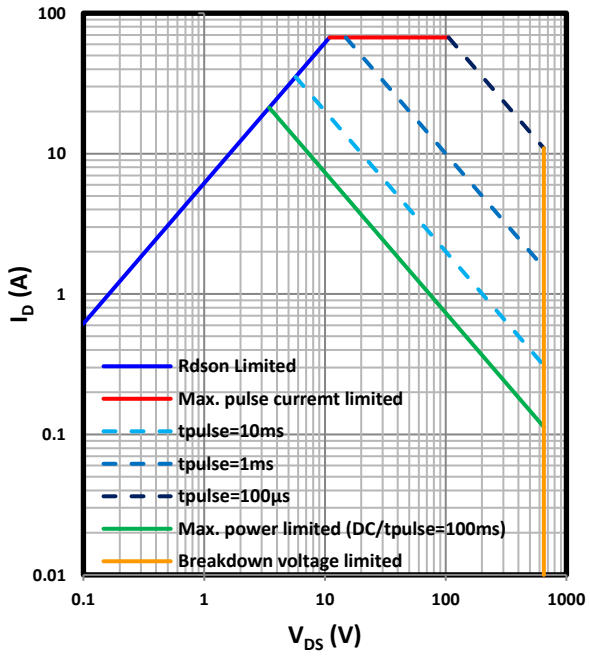
$P_{tot}=f(T_c)$

Fig 2. Max. transient thermal impedance



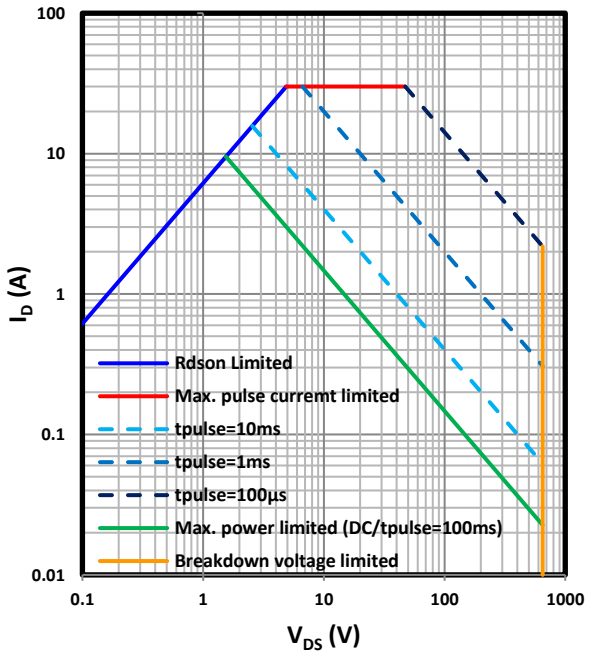
$Z_{thjc}=f(t_p, D)$

Fig 3. Safe operating area T_c=25°C



$I_D=f(V_{DS})$; Duty=0%; parameter: t_P

Fig 4. Safe operating area T_c=125°C



$I_D=f(V_{DS})$; Duty=0%; parameter: t_P

Confidential Level_ Public

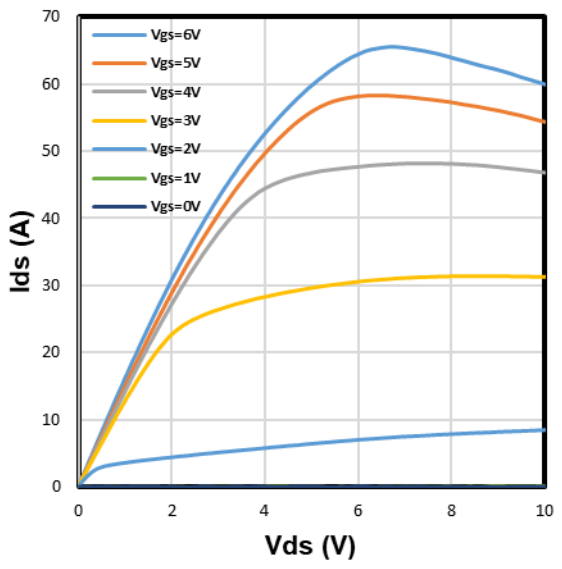
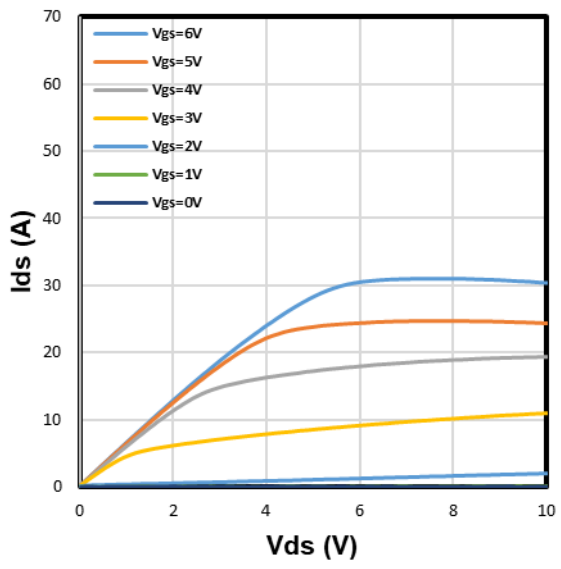
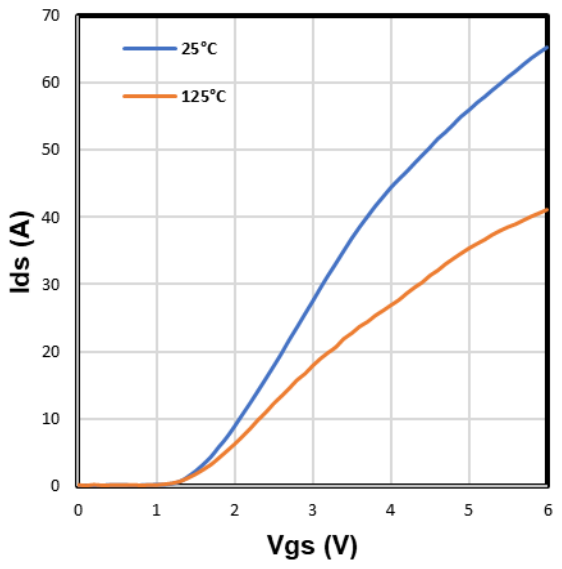
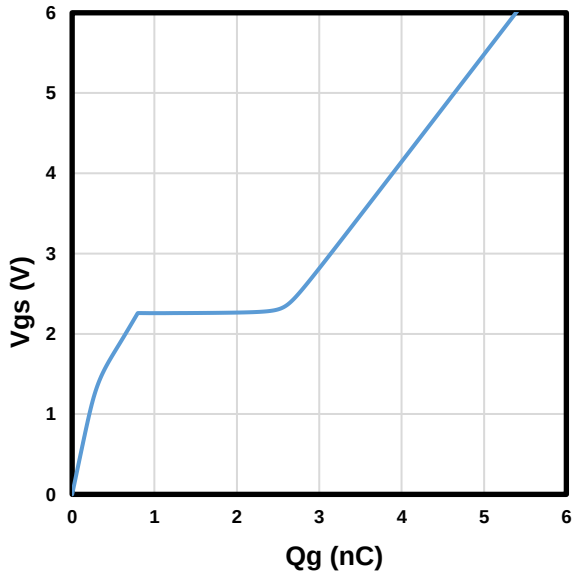
Fig 5. Typ. Output characteristics Tc=25°C	Fig 6. Typ. Output characteristics Tc=125°C
	
$I_D=f(V_{DS})$; T_j=25°C; parameter: V_{GS}	$I_D=f(V_{DS})$; T_j=125°C; parameter: V_{GS}

Fig 7. Typ. Transfer characteristics	Fig 8. Typ. Gate charge (Simulation)
	
$I_D=f(V_{GS})$; T_j=25 & 125°C; V_{DS}=10V	$V_{GS}=f(Q_G)$; V_{DC}=400V, I_D=8A

Confidential Level_ Public

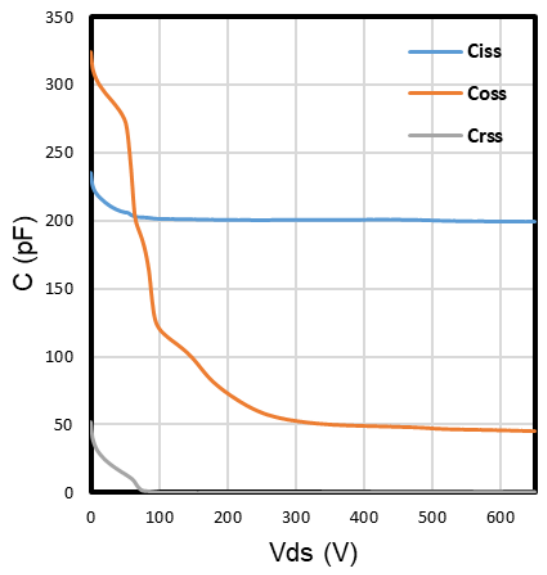
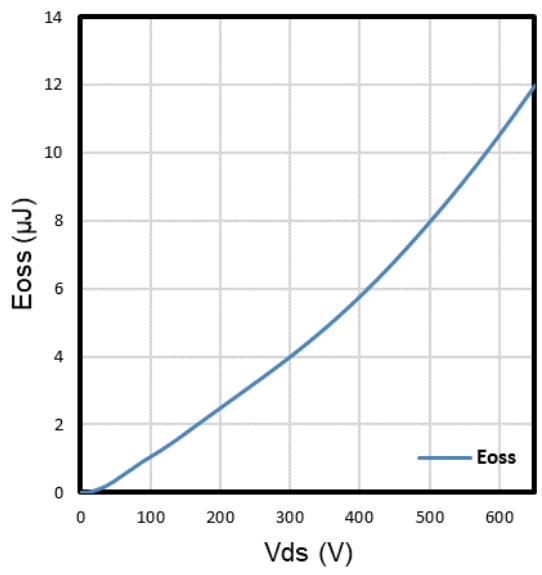
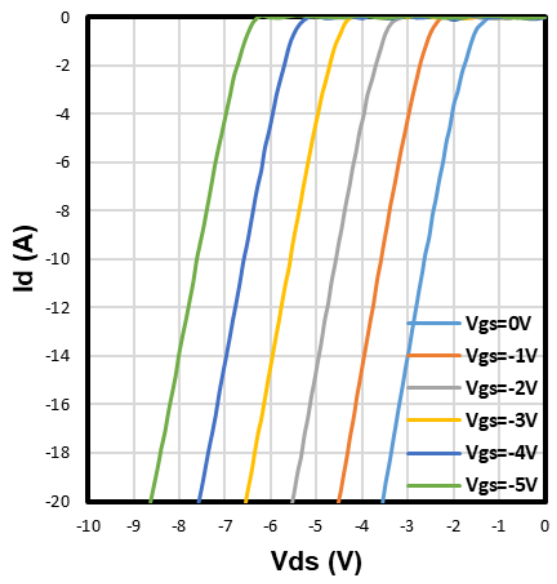
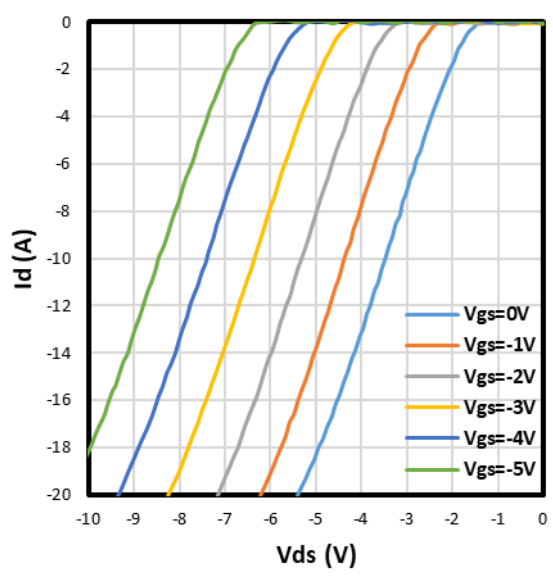
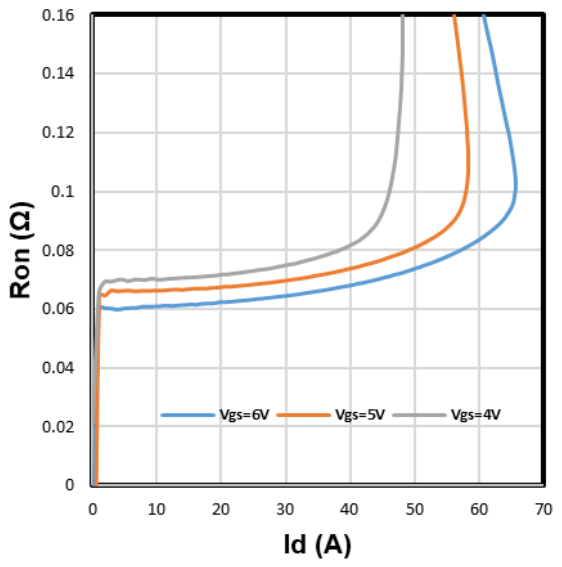
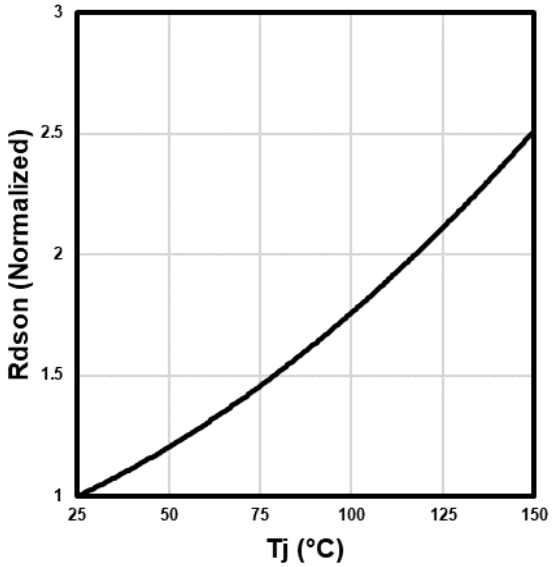
Fig 9. Typ. Capacitance	Fig 10. Typ. Coss stored energy
	
$C=f(V_{DS})$; V_{DS}=650V; parameter: T_j=25°C	$E_{oss}=f(V_{DS})$

Fig 11. Typ. channel reverse characteristics	Fig 12. Typ. channel reverse characteristics
	
$V_{DS}=f(V_{GS}, I_D)$; T_j=25°C	$V_{DS}=f(V_{GS}, I_D)$; T_j=125°C

Confidential Level_ Public

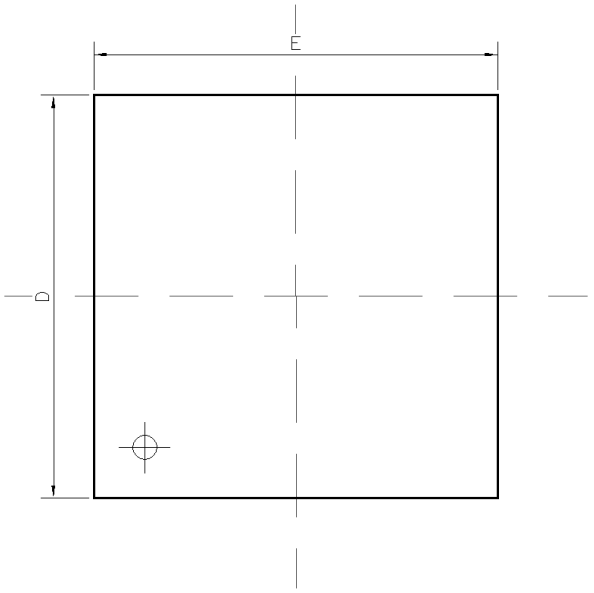
Fig 13. Typ. Drain-source on-state resistance	Fig 14. Typ. Drain-source on-state resistance
	
$R_{DS(on)}=f(I_D)$; $T_j=25°C$	$R_{DS(on)}=f(T_j)$; $I_D=8A$

Confidential Level_ Public

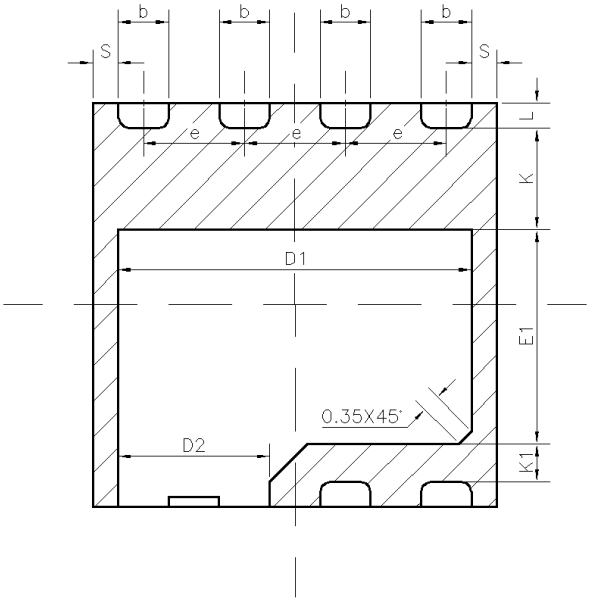
6. Package outlines

Package Name: DFN 8 x 8mm

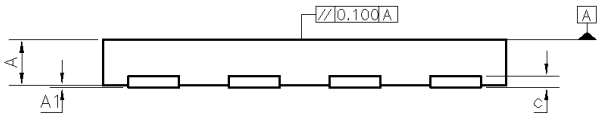
Top View

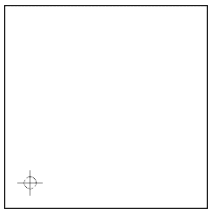


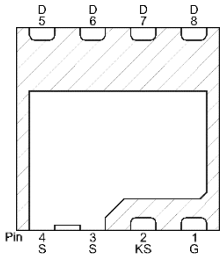
Bottom View



Side View



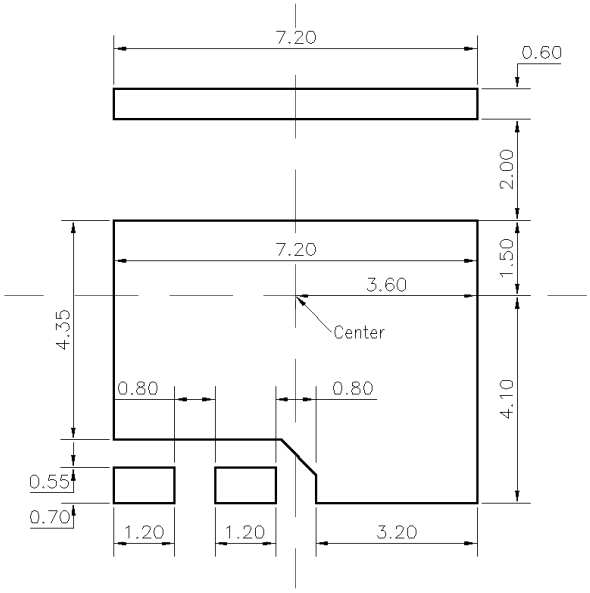


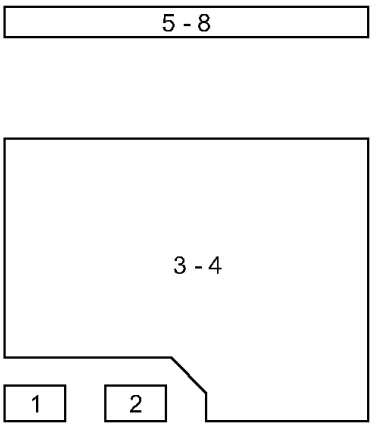


SYMBOLS	DIMENSIONS IN ILLMETERS		
	MIN.	NOM.	MAX.
A	0.75	0.85	0.95
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
C	0.20 REF		
D	7.90	8.00	8.10
D1	6.95	7.00	8.05
D2	2.95	3.00	3.05
E	7.90	8.00	8.10
E1	4.15	4.25	4.35
e	---	2.00	---
K	2.00 REF		
K1	0.75 REF		
L	0.45	0.50	0.55
S	0.45	0.50	0.55

Confidential Level_ Public

7. Footprint outlines

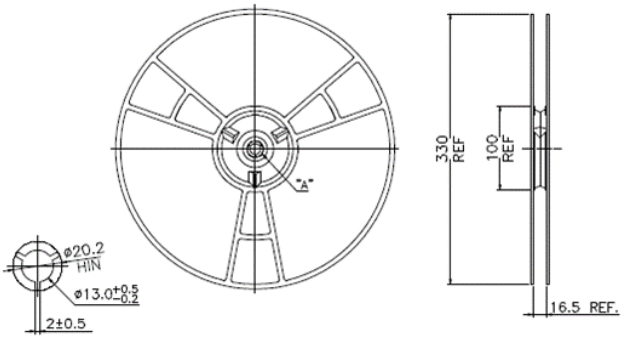


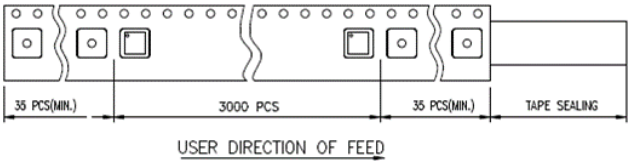


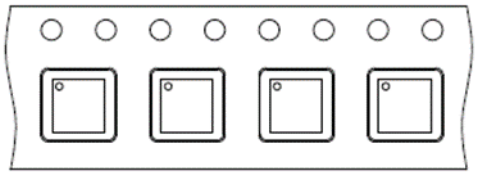
Pin No.	Terminal
1	Gate
2	Kelvin Source
3 - 4	Source
5 - 8	Drain

Confidential Level_ Public

8. Tape and reel configuration

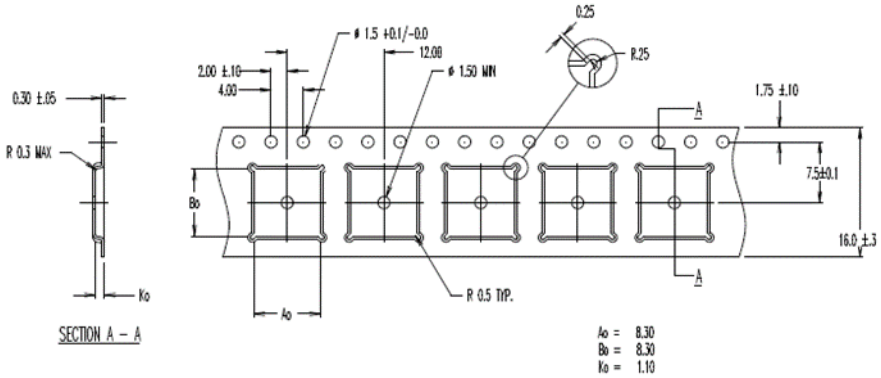






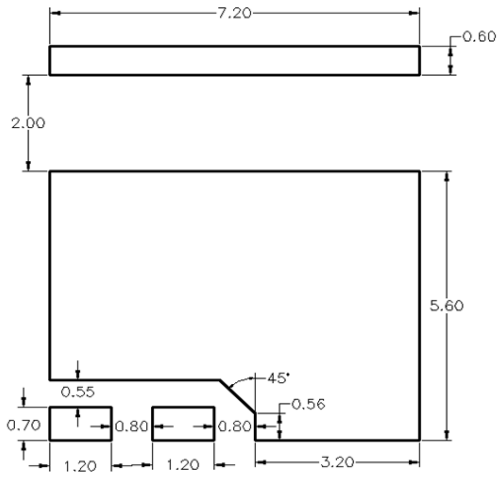
QFN 8X8

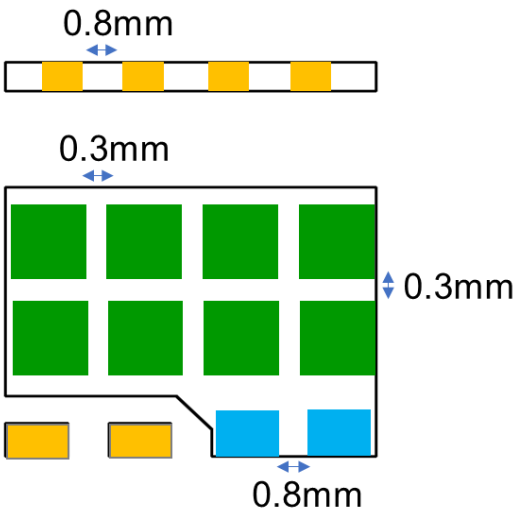
包装方式：3000 EA/PER REEL



Confidential Level_ Public

9. Stencil Recommended





Define the dimension of steel plate opening:

In this case,

thickness of steel plate : 100 um

the total area of the steel plate opening is about 50~60% on pad.

- 1.2 x 0.6 mm2
- 1.5 x 1.6 mm2
- 1.2 x 1.2 mm2

Confidential Level_ Public

ANCORA