GaN Enhancement Mode 650V Power Transistor

FET-E6007PD020

Datasheet Rev. V03

ANCORA

Confidential Level_ Public

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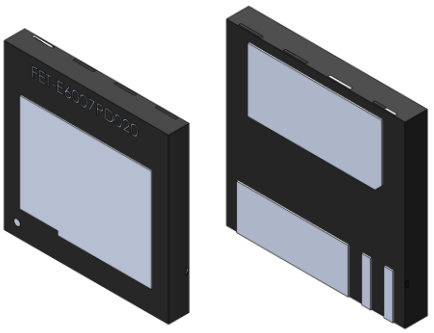
1. Description



Features

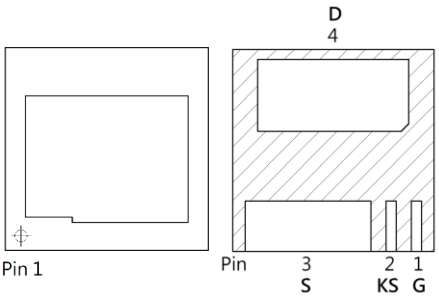
- 650V E-mode GaN FET
- DFN 8x8 mm (Double side cooling)

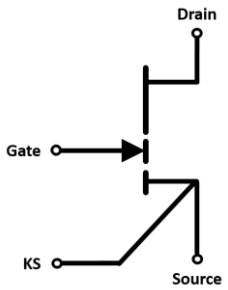
Applications

- High switching frequency converter
- High density converter

Table 1. Key Performance Parameters at T_j = 25°C

Parameter	Value	Unit
$V_{DS,\ max.}$	650	V
$R_{DS(on),\ typ.}$	60	mΩ
$Q_{G,\ typ.}$	5.02	nC
I_D Continuous drain current	38.3	A
Q_{oss} @ 400V	42.4	nC
Q_{rr}	0	nC
E_{oss} @ 400V	5.1	μJ





2. Maximum ratings

At T_j=25°C, unless otherwise specified.

Table 2. Maximum rating

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain source voltage	V_{DS}	-	-	650	V	V_{GS}=0V
Drain source pulse voltage [1)]	$V_{DS(pulse)}$	-	-	800	V	V_{GS}=0V, time≦1μs, T_j≦125°C, ≦10 million Pulses
Continuous drain current	I_D	-	-	38.3	A	T_C=25°C, T_j=150°C
		-	-	24.2	A	T_C=100°C, T_j=150°C
		-	-	17.1	A	T_C=125°C, T_j=150°C
Pulsed drain current	$I_{D,\ pulse}$	-	-	121.6	A	T_C=25°C, V_{GS}=6V (Duty=0.1, t_{pulse}=1μs) See Fig. 3
		-	-	54.4	A	T_C=125°C, V_{GS}=6V (Duty=0.1, t_{pulse}=1μs) See Fig. 4
Gate source voltage	V_{GS}	-10	-	7	V	Recommended operating Range: V_{GS} >=5.5V
Gate source pulse voltage	$V_{GS(pulse)}$	-	-	8.5	V	time=20ns, T_j≦125°C, ≦10 million Pulses
Power dissipation	P_{tot}	-	-	176	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	Max shelf life depends on storage conditions
Operating junction temperature	T_j	-55	-	150	°C	-
Drain source voltage slew rate	dV/dt	-	-	200	V/ns	-

[1)] The allowable non-periodic VDS_pulse under abnormal operating conditions should be below 800V.
The operation for pulse number≤10 million cycles has been checked.

3. Thermal characteristics

Table 3. Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC_top}	-	0.71	-	°C/W	Top case
	R_{thJC_bottom}	-	2.92	-	°C/W	Bottom case
Thermal resistance, junction-ambient for SMD version	R_{thJA}	-	45	-	°C/W	Device on 40x40x1.5mm3 single layer epoxy PCB FR4 with 6cm2 copper area (2oz.). PCB is vertical in still air.
Soldering temperature, wave soldering only allowed at leads	T_{solder}	-	-	260	°C	MSL3

4. Electrical characteristics

At T_j=25°C, unless otherwise specified.

Table 4. Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.0	1.6	2.6	V	V_{DS}=50mV, I_D=16mA, T_j=25°C
Drain-source leakage current	I_{DSS}	-	0.17	168	μA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
		-	40	-	μA	V_{DS}=650V, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	30	-	μA	V_{GS}=6V, V_{DS}=0V, T_j=25°C
Drain-source on-state resistance	$R_{DS(on)}$	-	56	-	mΩ	V_{GS}=5.5V, I_D=8A, T_j=25°C
		-	60	89	mΩ	V_{GS}=6V, I_D=8A, T_j=25°C
		-	59	-	mΩ	V_{GS}=6.5V, I_D=8A, T_j=25°C
		-	120	-	mΩ	V_{GS}=6V, I_D=8A, T_j=150°C
Source-drain reverse voltage	V_{SD}	-	2.82	-	V	V_{GS}=0V, I_D=8A, T_j=25°C

Table 5. Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	155.3	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
Output capacitance	C_{oss}	-	38.3	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
Reverse transfer capacitance	C_{rss}	-	0.61	-	pF	V_{GS}=0V, V_{DS}=400V, f=1MHz
Effective output capacitance, energy related [2]	$C_{o(er)}$	-	63.7	-	pF	V_{GS}=0V, V_{DS}=0V to 400V
Effective output capacitance, time related [3]	$C_{o(tr)}$	-	106	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0V to 400V
Output charge	Q_{oss}	-	42.4	-	nC	V_{GS}=0V, V_{DS}=0 to 400V
Turn-on delay time [4]	$t_{d(on)}$	-	3.36	-	ns	V_{DS}=400V, V_{GS}=6V/-1.5V, I_D=8A, R_G=5Ω
Rise time [4]	t_r	-	3.9	-	ns	V_{DS}=400V, V_{GS}=6V/-1.5V, I_D=8A, R_G=5Ω
Turn-off delay time [4]	$t_{d(off)}$	-	8.76	-	ns	V_{DS}=400V, V_{GS}=6V/-1.5V, I_D=8A, R_G=5Ω
Fall time [4]	t_f	-	5.6	-	ns	V_{DS}=400V, V_{GS}=6V/-1.5V, I_D=8A, R_G=5Ω
Gate resistance	R_G	-	1.6	-	Ω	f=100MHz, open drain

[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.

[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V.

[4] Test circuit:

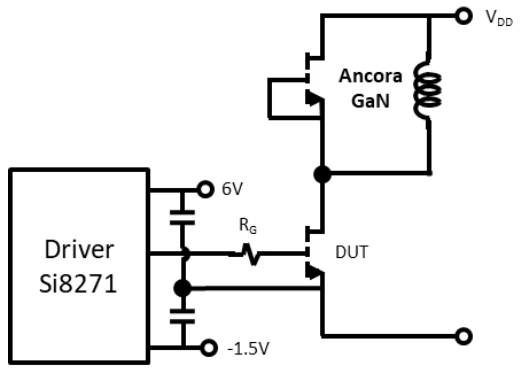


Table 6. Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	0.79	-	nC	V_{DS}=400V, I_D=8A, V_{GS}=0 to 6V
Gate to drain charge	Q_{GD}	-	1.95	-	nC	V_{DS}=400V, I_D=8A, V_{GS}=0 to 6V
Gate charge total	Q_G	-	5.02	-	nC	V_{DS}=400V, I_D=8A, V_{GS}=0 to 6V
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	V_{DS}=400V, I_D=8A, V_{GS}=0 to 6V

Table 7. Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Pulsed current, reverse	$I_{s,\ pulse}$	-	-	121.6	A	Tc=25°C
Reverse recovery chart	Q_{rr}	-	0	-	nC	Excluding Qoss
Reverse recovery time	T_{rr}	-	0	-	nS	-
Peak reverse recovery current	I_{rrm}	-	0	-	A	-

5. Electrical characteristics diagrams

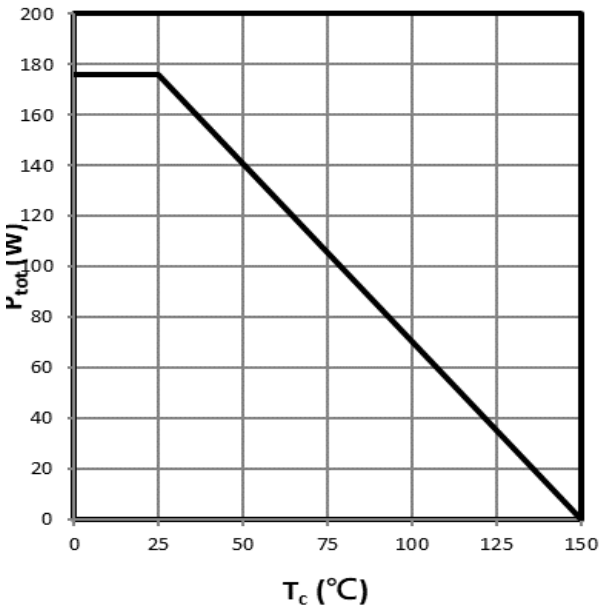
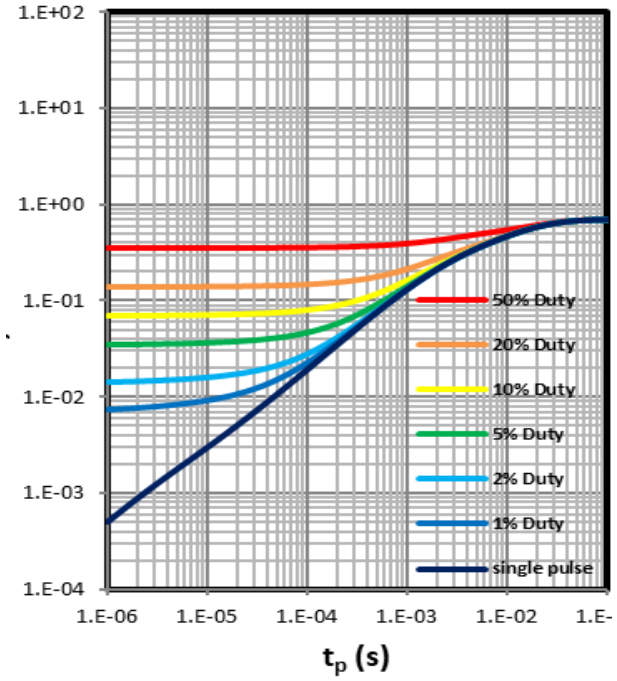
Fig 1. Power dissipation	Fig 2. Max. transient thermal impedance
	
$P_{tot}=f(T_c)$	$Z_{thjc}=f(t_p, D)$

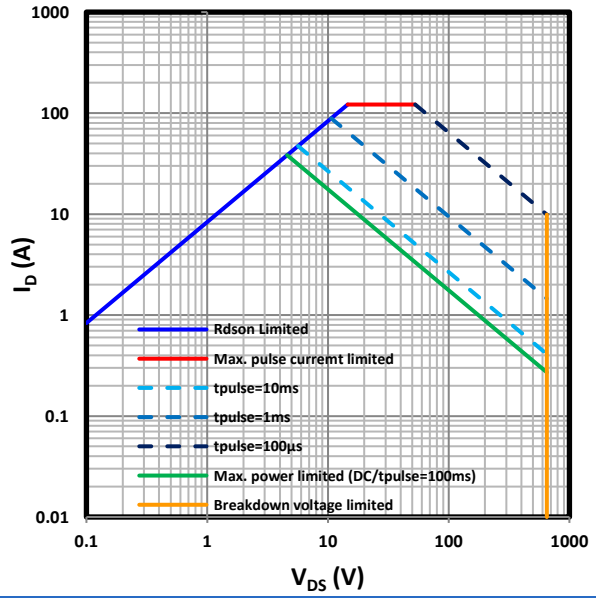
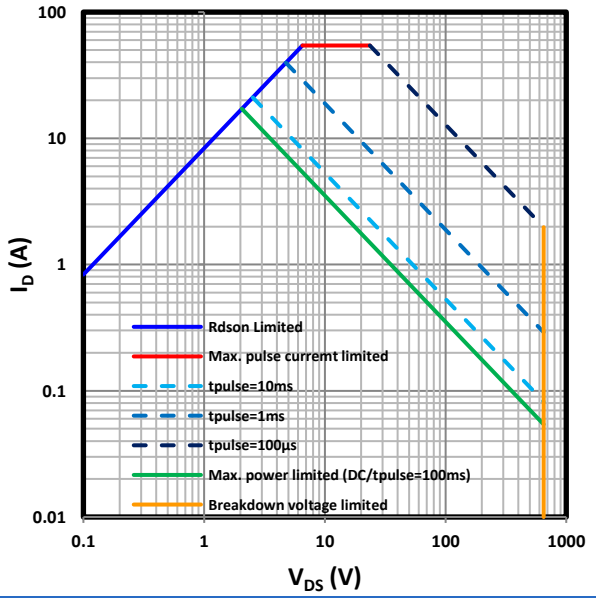
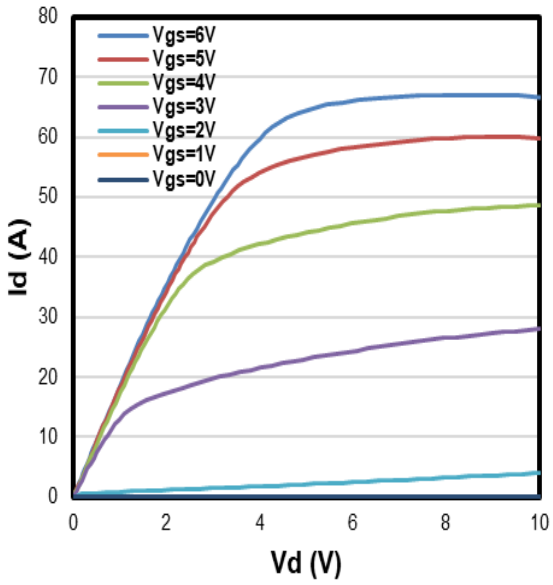
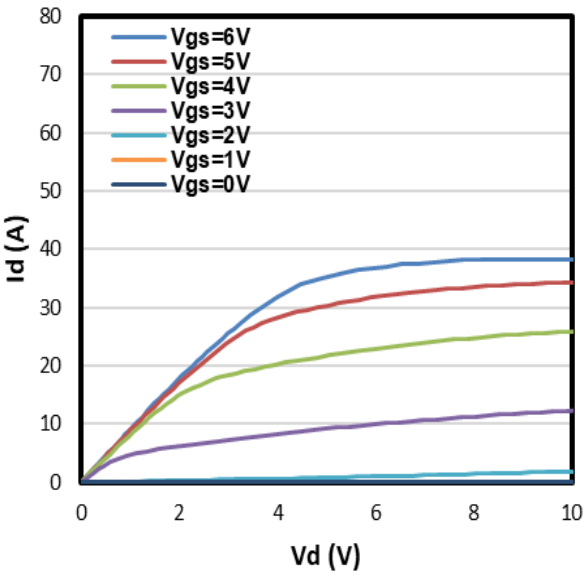
Fig 3. Safe operating area T_c=25°C	Fig 4. Safe operating area T_c=125°C
	
$I_D=f(V_{DS})$; Duty=0%; parameter: t_P	$I_D=f(V_{DS})$; Duty=0%; parameter: t_P

Fig 5. Typ. Output characteristics Tc=25°C



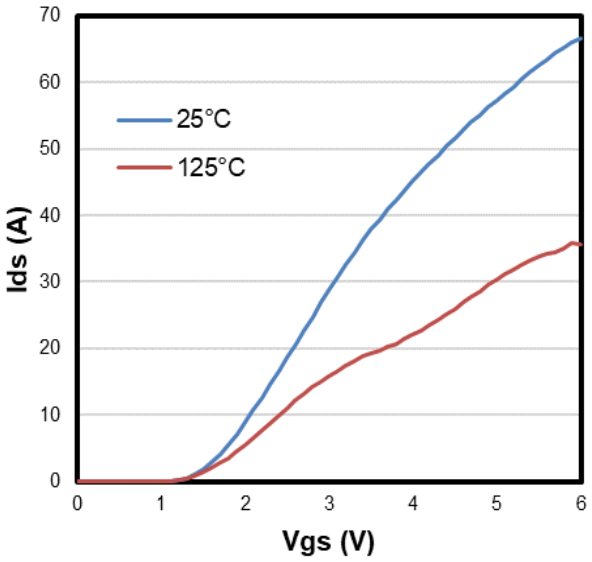
$I_D=f(V_{DS})$; $T_j=25°C$; parameter: V_{GS}

Fig 6. Typ. Output characteristics Tc=125°C



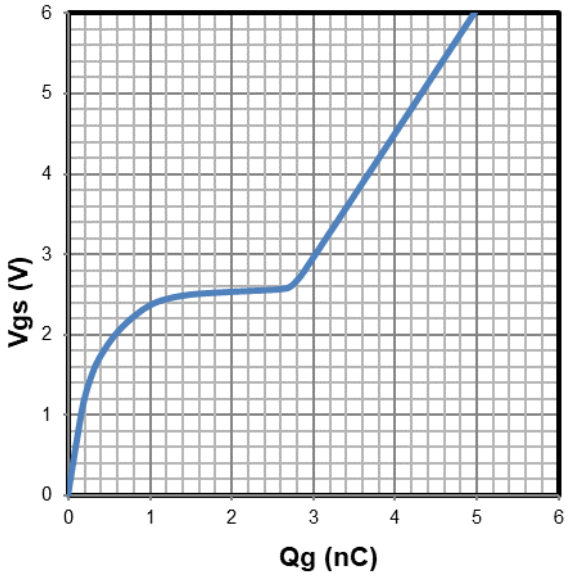
$I_D=f(V_{DS})$; $T_j=125°C$; parameter: V_{GS}

Fig 7. Typ. Transfer characteristics



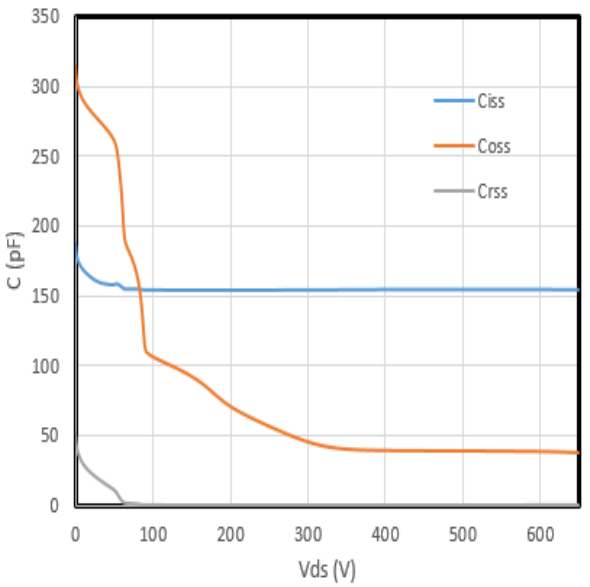
$I_D=f(V_{GS})$; $T_j=25$ & $125°C$; $V_{DS}=10V$

Fig 8. Typ. Gate charge (Simulation)



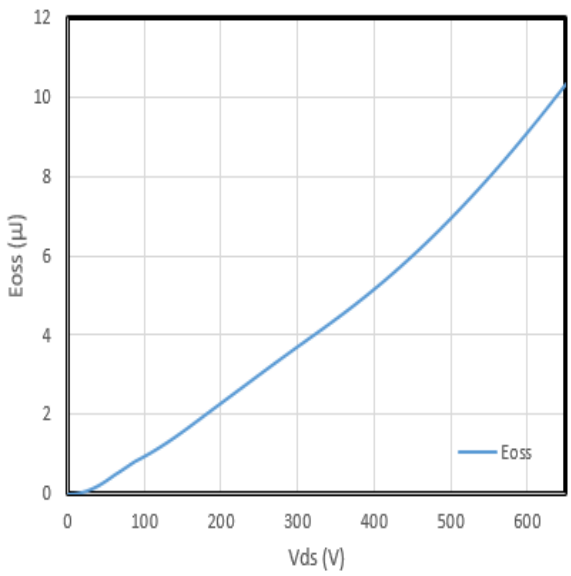
$V_{GS}=f(Q_G)$; $V_{DC}=400V$, $I_D=8A$

Fig 9. Typ. Capacitance



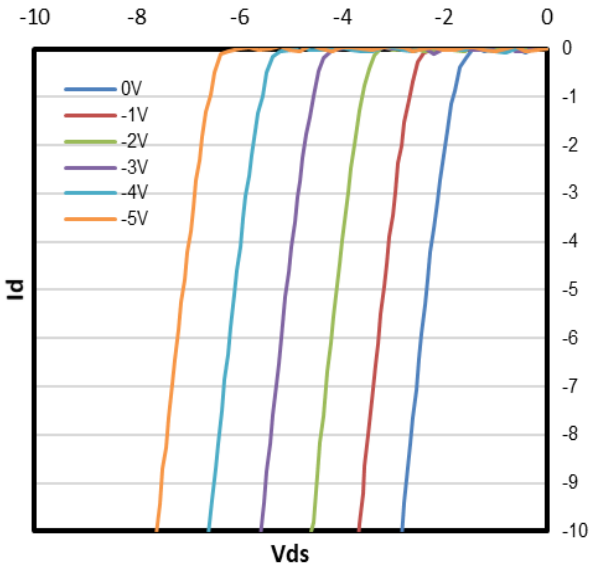
$C=f(V_{DS})$; V_{DS}=650V; parameter: T_j=25°C

Fig 10. Typ. Coss stored energy



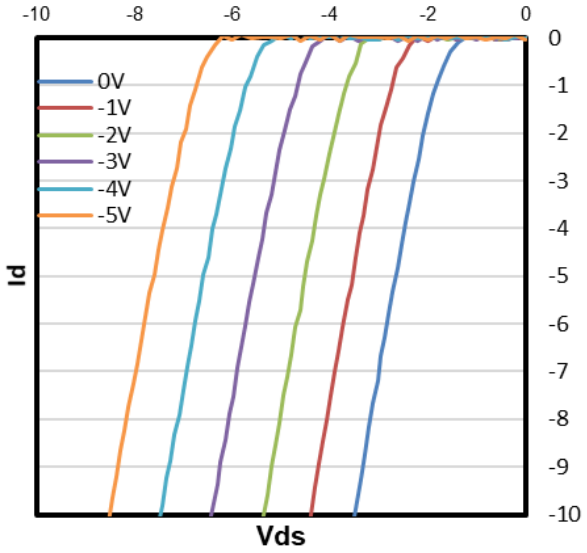
$E_{oss}=f(V_{DS})$

Fig 11. Typ. channel reverse characteristics



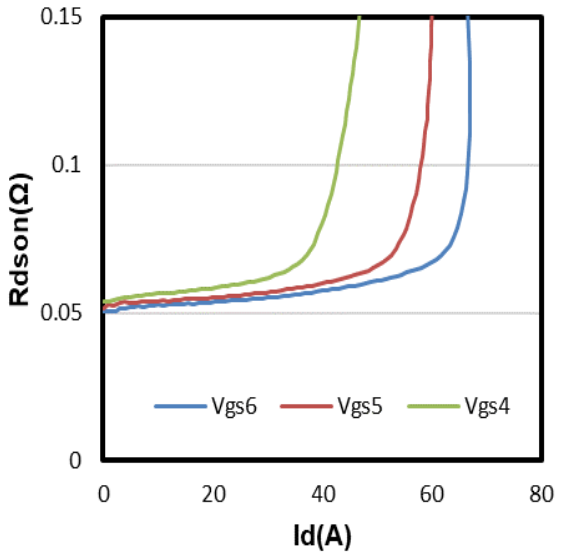
$V_{DS}=f(V_{GS,}\ I_D)$; T_j=25°C

Fig 12. Typ. channel reverse characteristics



$V_{DS}=f(V_{GS,}\ I_D)$; T_j=125°C

Fig 13. Typ. Drain-source on-state resistance

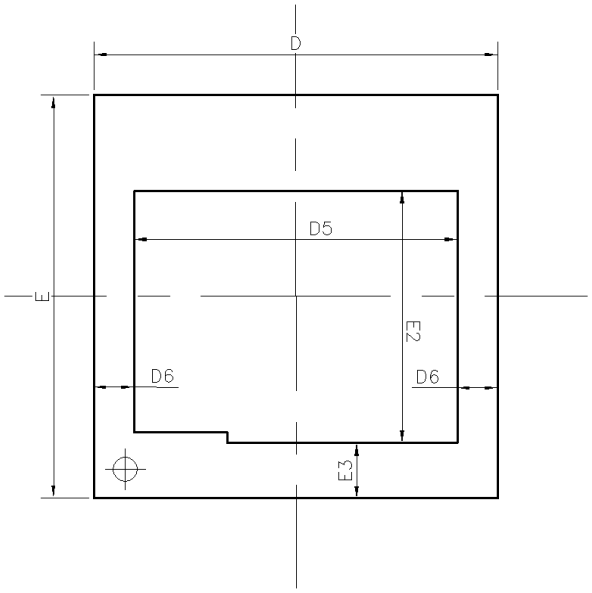


$R_{DS(on)}=f(I_D)$; $T_j=25°C$

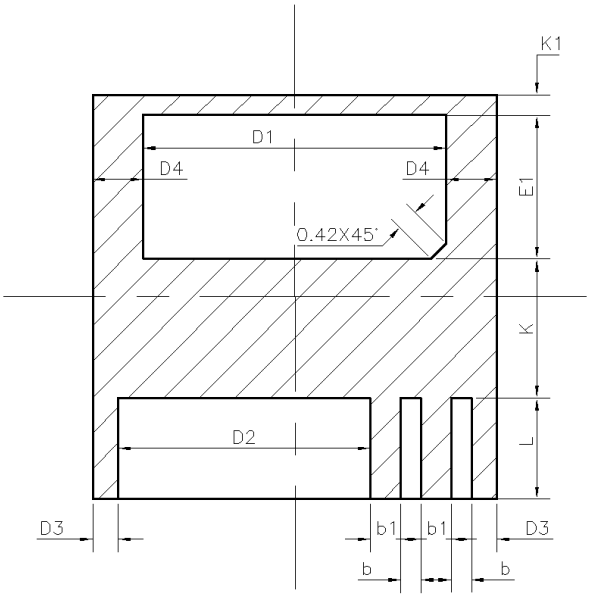
6. Package outlines

Package Name: DFN 8 x 8mm (Double Side Cooling)

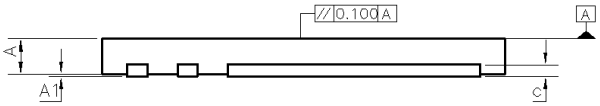
Top View

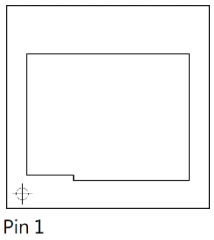


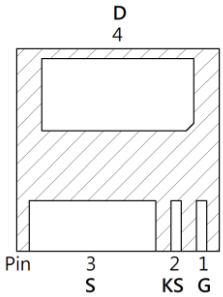
Bottom View



Side View

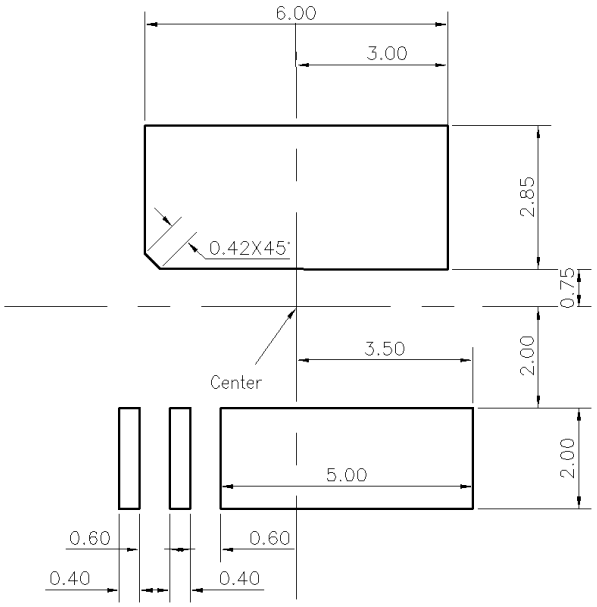


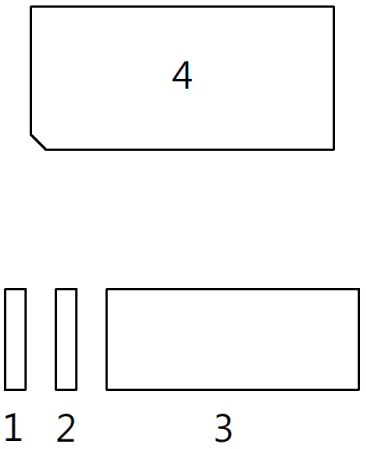




SYMBOLS	DIMENSIONS IN MILLMETERS		
	MIN.	NOM.	MAX.
A	0.95	1.05	1.15
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
b1	0.55	0.60	0.75
C	---	0.20 REF	---
D	7.90	8.00	8.10
D1	5.90	6.00	6.10
D2	4.90	5.00	5.10
D3	0.40	0.50	0.60
D4	0.90	1.00	1.00
D5	6.20	6.40	6.60
D6	0.60	0.80	1.00
E	7.90	8.00	8.10
E1	2.75	2.85	2.95
E2	4.80	5.00	5.20
E3	0.90	1.10	1.30
K	2.65	2.75	2.85
K1	0.30	0.40	0.50
L	1.90	2.00	2.10

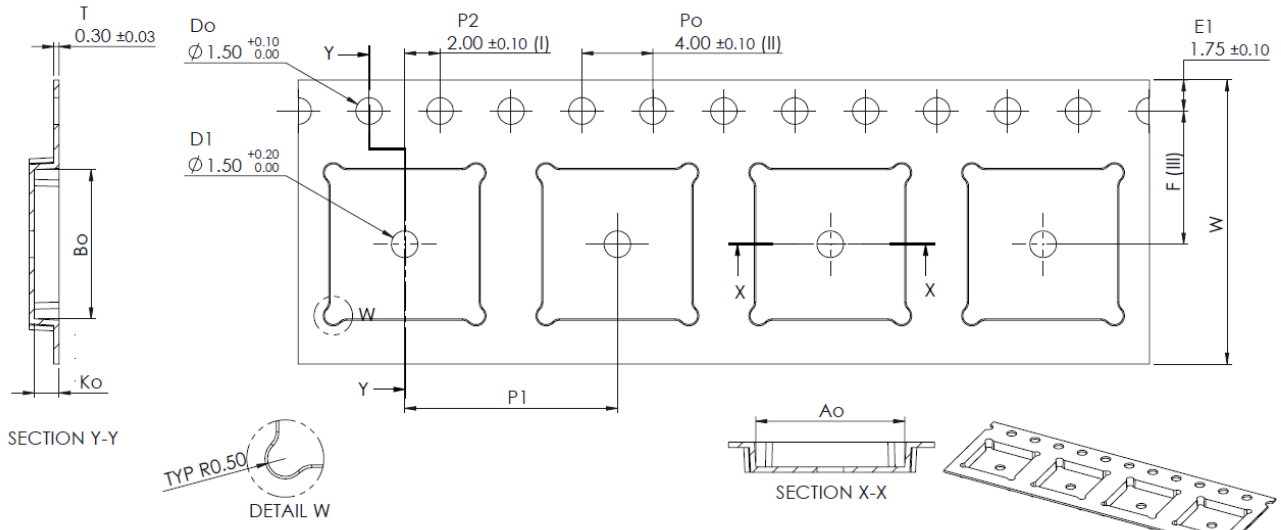
7. Footprint outlines





Pin No.	Terminal
1	Gate
2	Kelvin Source
3	Source
4	Drain

8. Tape and reel configuration



Ao	8.40	+/- 0.10
Bo	8.40	+/- 0.10
Ko	1.40	+/- 0.10
F	7.50	+/- 0.10
P1	12.00	+/- 0.10
W	16.15	+/- 0.10

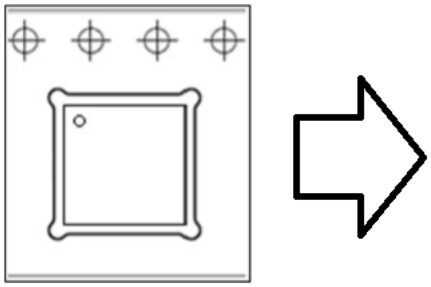
Comply to EIA-481-E	Customer Confirmation for Tool-up
	Approved by:
Tooling Code : 17-B Estimated length : 500m/22X10CY(96mm)reel	Date:

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

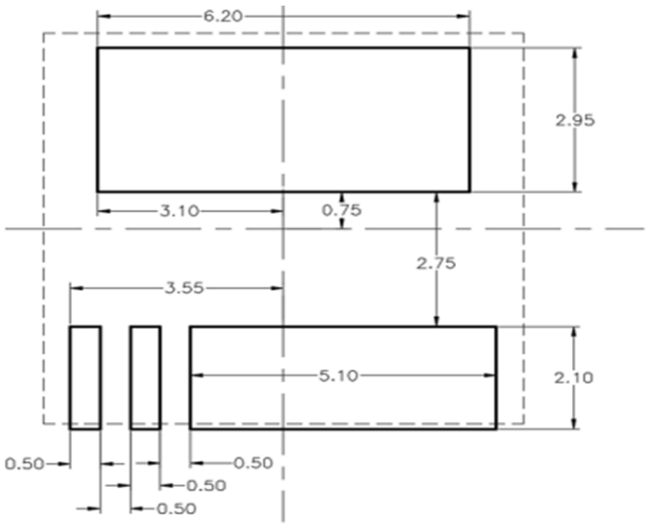
ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

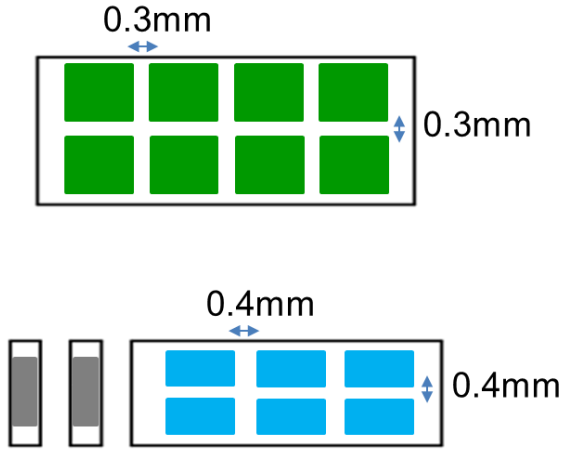
3500 EA / Per Reel

Pin1 Direction



9. Stencil Recommended





Define the dimension of steel plate opening:

In this case,

Thickness of steel plate: 100 um

The total area of the steel plate opening is about 50~60% on pad.

- 1.2 x 1.2 mm2
- 0.5 x 1.7 mm2
- 1.2 x 0.7 mm2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